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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,140	03/15/2001	William E. Corr	M4065.0424/P424	4623

24998 7590 08/19/2004

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EXAMINER	
DEB, ANJAN K	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,140	CORR, WILLIAM E.	
	Examiner	Art Unit	
	Anjan K Deb	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-33,35-47,49-53,55-76 and 78-98* is/are pending in the application.

4a) Of the above claim(s) *53,55-76 and 78-98* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,12-19,22-28,31-33,35-42,45,50 and 51* is/are rejected.

7)☒ Claim(s) *6-11,20,21,29,30,43,44,46,47,49 and 52* is/are objected to.

8)☒ Claim(s) *1,3-33,35-47,49-53,55-76 and 78-98* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-5, 12-14, 17-19, 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasui et al. (US 4,278,971).

Re claim 1, Yasui et al. discloses (Fig. 1) method for measuring a parameter of a circuit under test 5, comprising charging a first portion 6 of test circuit up to a first voltage level (voltage at node A), charging a second portion 10 of said test circuit up to a second voltage level (voltage at node B), disconnecting (switch 1a open) test circuit 5 from respective voltage terminals providing first and second voltage levels, and measuring (18)(indicating lamp) parameter (High or Low level) of circuit under test 5 with test circuit.

Re claims 3-5, Yasui et al. discloses charging a first portion comprises charging a first capacitor 6 of said test circuit to a power rail voltage level (voltage at node A is considered rail voltage), and wherein said act of charging a second portion comprises charging a second capacitor 10 of said test circuit to a predetermined reference voltage level.

Re claims 12-14, Yasui et al. discloses disconnecting test circuit from power rail (switch 1a open).

Re claims 17, 19, Yasui et al. discloses act of measuring comprises comparing a sensed voltage with a reference voltage. Voltage at node B is considered reference voltage.

Re claim 18, Yasui et al. discloses act of comparing comprises comparing voltage sensed at a ground terminal (node C) of said circuit under test with a reference voltage.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al. (US 4,278,971) in view De Jong (US 6,664,798).

Re claims 22, 23 Yasui et al. discloses all of the claimed limitations as set forth above except quantifying ground bounce and quantifying power droop of circuit under test.

De Jong et al. disclose test circuit for testing integrated circuit comprising quantifying ground bounce and power droop for said circuit under test.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yasui et al. by adding comparator with variable threshold disclosed by De Jong et al. for quantifying ground bounce and power droop for said circuit under test.

5. Claims 15, 16, 24-28, 31, 32, 35-41, 45, 49, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al. (US 4,278,971) in view of Frech et al. (US 2002/0125897).

Re claims 15, 16, 24-28, 31, 32, 35, 36, 40 Yasui et al. discloses all of the claimed limitations as set forth above except respective switches within first and second charging portions for disconnecting test circuit from terminals respectively providing said first and second voltage levels.

Frech et al. discloses method of quantifying on-chip power supply integrity comprising disconnecting 102 test circuit C_s from terminals respectively providing said first and second voltage levels. Switch 102 is broadly interpreted as transistor switch.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yasui et al. by adding a transistor switch (switching capacitor) disclosed by Frech et al. for disconnecting test circuit from terminals respectively for testing on-chip power supply integrity.

Re claim 36, Yasui et al. disclose comparator 12 comprises an output for producing a signal when said parameter, as measured, has a predetermined relationship with a reference voltage.

Re claim 37, Yasui et al. did not expressly disclose test circuit is integrated onto a semiconductor die.

Frech et al. discloses method of quantifying on-chip power supply integrity comprising integrated circuits. Integrated circuit is broadly interpreted as semiconductor die.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yasui et al. by adding test circuit integrated onto a semiconductor die for testing on-chip power supply integrity.

Re claims 38, 39, Yasui et al. discloses all of the claimed limitations including charging first 10 and second 6 circuit portion to first and second voltage level respectively, except respective switches within first and second circuit portion.

Frech et al. discloses method of quantifying on-chip power supply integrity comprising respective switches 102 within first and second circuit portions (partitions)(page 3 para 0028).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yasui et al. by adding respective switches disclosed by Frech et al. for testing on-chip power supply of each partitioned circuit.

Re claim 41 Yasui et al. discloses measuring portion comprises a comparator 12.

Re claim 45 Yasui et al. discloses second input of comparator 12 coupled to terminal A providing second voltage level, said terminal being reference voltage terminal for providing a reference voltage, said comparator comparing said reference voltage and said sensed parameter (voltage at node B) of said at least one circuit to be tested.

Re claim 49, Yasui et al. discloses second charging portion comprises a second storage capacitor 10 for providing said reference voltage to said second input (node B) when said second input is disconnected (switch 1a open) from said reference voltage terminal.

Allowable Subject Matter

6. Claims 6-11, 20, 21, 29, 30, 43, 44, 46, 47, 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gillund (US 3,629,816) discloses monitoring circuit comprising first and second charging capacitors and monitoring voltage level after disconnecting voltage supply to circuit (Fig. 1).

Frech (US 6,424,058 B1) discloses method of testing on-chip power supply by charging capacitor (Fig. 2).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le, can be reached at (571) 272-2233.

Anjan K. Deb
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8/5/04

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